Write your name at the top right corner of every page (including this cover page).

Copy everything you want counted towards your grade onto the pages that I provided.

Write with a pen that cannot be erased!

No books or calculators are allowed!

Write down all the steps that lead to your result.

Identify new variables that you may introduce in the circuit diagrams that I provided or you draw yourself.

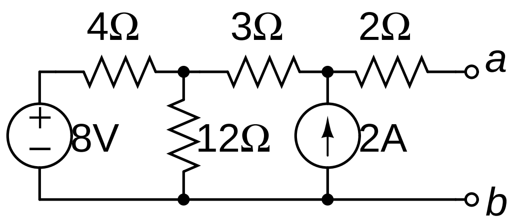
Read all the problems before you start so that you can begin with those that seem easiest to you.

The last problem is for the Graduate level students only. Undergraduates that solve this problem may substitute it for another problem. The points earned will be scaled to the total of the problem that was replaced. If that problem is solved by an undergraduate and sufficient points are earned, I will choose the problem to be replaced such as to optimize the total points.

This is the solutions version

Problem 1 (6 pts):

Find the Thevenin equivalent circuit for the circuit shown below. If you connect a load resistor R_L between the terminals *a* and *b*: What value of R_L will allow for the maximum power transfer to the load?

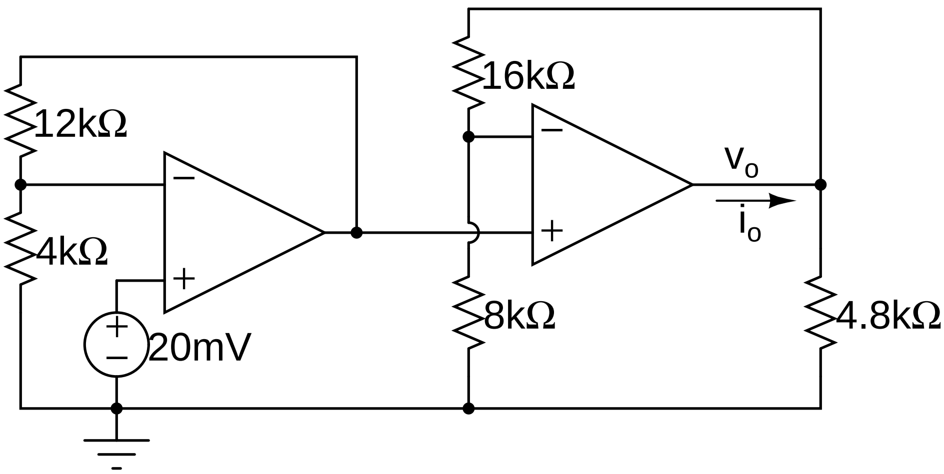


Solution:

To get the Thevenin resistance we short out the voltage source and break the connection through the current source. The 4Ω and the 12Ω are in parallel then and as such in series with the 3Ω and the 2Ω resistors:
$R_{Th} = 3\Omega + 2\Omega + \frac{4\Omega 12\Omega}{4\Omega + 12\Omega} = 8\Omega$
To get the Thevenin voltage, we apply mesh analysis to the open circuit as shown in the problem, with nothing connected to the outputs a and b. If we call i_1 (left) and i_2 (right) the clockwise currents around the two meshes in the circuit, we write:
$-8V + 4\Omega i_1 + 12\Omega(i_1 - i_2) = 0$ and $i_2 = -2A$,
which yields: $i_1 = -1A$.
This means that the open circuit voltage between a and b is:
$U_{Th} = 12\Omega(i_1 - i_2) - 3\Omega i_2 = -12V + 24V + 6V = 18V$
For maximum power transfer to the load $R_L = R_{Th}$.

Problem 2 (6 pts):

Calculate v_o and i_o in the circuit below.



Solution:

There are two non-inverting amplifier stages in this circuit. The first one will put out:
$v_1 = (1 + \frac{12k\Omega}{4k\Omega})20\text{mV} = 80\text{mV}$
This being the input to the second stage, we get for the second stage's output: $v_o = (1+\frac{16k\Omega}{8k\Omega})80\text{mV} = 240\text{mV}$
No current is coming out or drained into the Op-Amp input:
$i_o = \frac{240\text{mV}}{16k\Omega+8k\Omega} + \frac{240\text{mV}}{4.8k\Omega} = 60\mu\text{A}$

Problem 3 (6 pts):

Write the Karnaugh map and analyze it to find an efficient(!) implementation for the following truth table:

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Solution:

AB-CD	00	01	11	10
00	1	1	0	1
01	1	1	1	1
11	1	1	0	1
10	1	1	0	0

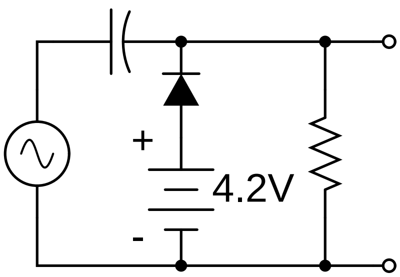
Be sure to get the order right: Only one bit changing between rows or columns!

$F = \overline{C} + \overline{A}B + \overline{A}\,\overline{D} + B\overline{D}$

Problem 4 (4 pts):

Design a circuit that clamps the negative peaks of an ac signal to +3.6 V. Allow for 0.6 V forward voltage drop across your diode.

Solution:



Problem 5 (6 pts):

Use only the straight-line asymptotes to sketch the Bode Plot (both, amplitude and phase!) for the transfer function:

$H(j\omega) = (\frac{1}{1+j\omega})(\frac{j\omega}{10+j\omega})$

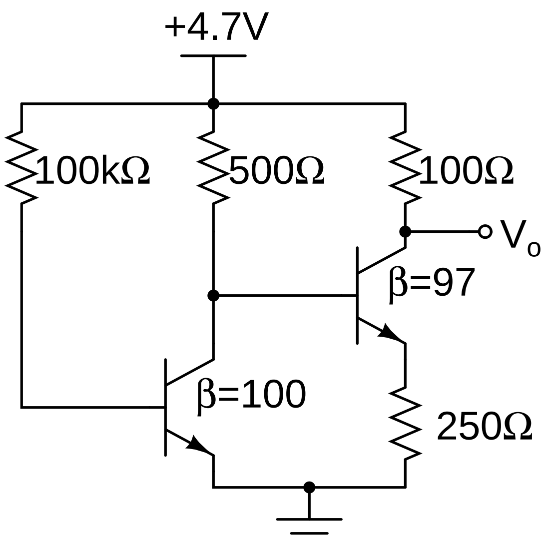
What type of filter is this?

Solution:

It is a band-pass filter with a maximum yield of -20dB. The amplitude plot comes up through $s = j\omega =$0.1 at -40dB to -20dB at 1.0, stays at -20dB until 10, and there turns back down through -40dB at 100. The phase stays at +90deg below $s =$0.1, drops to +45deg by 1.0, drops stronger now to -45deg by 10, and reaches -90deg at 100, where it stays for the higher frequencies.

Problem 6 (6 pts):

In the following setup you will find that both transistors are biased in the active region. Verify that and determine the output voltage V_o.

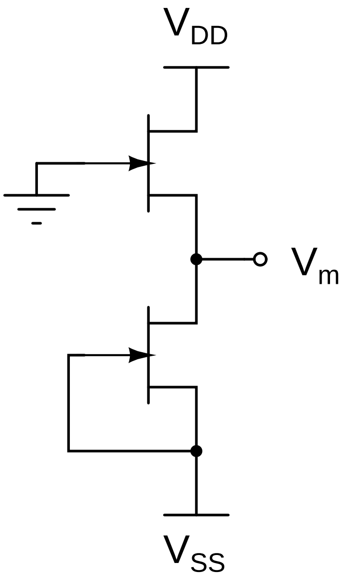


Solution:

Let me use the index 1 for quantities pertaining to the transistor with $\beta = 100$ and the index 2 for those pertaining to the transistor with $\beta = 97$. The base current i_{B1} is readily found: $i_{B1} = (4.7\text{V} - 0.7\text{V})/100\text{k}\Omega = 40\mu\text{A}$, implying $i_{C1} = 4\text{mA}$. We find i_{B2} by KVL:
$4.7\text{V} - 0.7\text{V} = 4\text{V} = 500\Omega(\text{i}_{\text{B2}} + \text{i}_{\text{C1}}) + 250\Omega(97 + 1)\text{i}_{\text{B2}}$
$4\text{V} - 500\Omega 4\text{mA} = 2\text{V} = 500\Omega\text{i}_{\text{B2}} + 250\Omega 98\text{i}_{\text{B2}}$
$2\text{V}/250\Omega = 8\text{mA} = 2\text{i}_{\text{B2}} + 98\text{i}_{\text{B2}} = 100\text{i}_{\text{B2}} \Rightarrow \text{i}_{\text{B2}} = 80\mu\text{A}$
Thus the voltage drop across the 100Ω resistor is $97 \times 80\mu\text{A} = 0.776\text{V} \approx 0.78\text{V}$. That gives $V_o \approx 3.92\text{V}$ and means that $v_{CE2} > 3.92\text{V} - 250\Omega 8\text{mA} = 1.92\text{V}$, i.e. active. Also: $v_{CE1} > 4.7\text{V} - 500\Omega 4.1\text{mA} = 2.2\text{V}$, i.e. active.

Problem 7 ONLY 6610 students !!! (6 pts):

In the following circuit both JFETs have $I_{DSS} = 4\text{mA}$ and $V_P = -2V$. The supply voltages are $V_{DD} = -V_{SS} = +10\text{V}$. Show that both JFETs are in the active region and determine V_m.



Solution:

For the lower of the two JFETs we know that $v_{GS} = 0V$ and therefore $i_D = I_{DSS} = 4\text{mA}$. This current flows through both JFETs, so the upper one must have $v_{GS} = 0V$ too. Its source therefore is at the same potential as its gate: V_m =GND. Now we know the situation is completely symmetric and it is sufficient to show that one of the two JFETs is in the active region: $v_{DS} = 10\text{V} > \text{v}_{\text{GS}} - \text{V}_{\text{P}} = 2\text{V}$, qed.