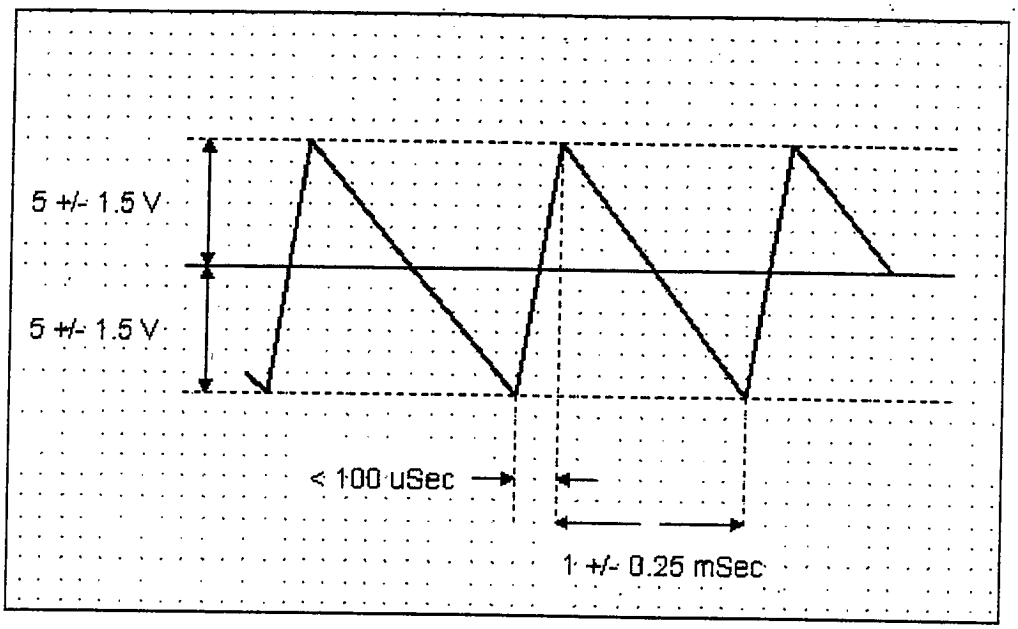
SESSION 23: A Sawtooth Waveform Generator

Construct a negative sawtooth waveform generator that will produce the following output:



SESSION 26: Frequency Synthesis With The Phase Locked Loop

In this Lab we will gain a bit of experience with the phase locked loop in a narrow bandwidth situation and with its use in generating signals related in frequency by a rational multiplier to an input frequency.

Using the breadboard 1 kHz signal as a "stable" standard, use the 565 phase locked loop to generate a stable 666 2/3 Hz output. Remember that a square wave has only odd harmonics. Again you benefit from the use of the ± 6 volt supplies for the 565. Standard CMOS circuitry without level shifting can be used for the necessary. frequency division. Use a potentiometer to control the 565 VCO free running frequency.

When the circuit is operating properly, the 666 2/3 Hz output will be "rock-steady" with respect to the 1 kHz reference signal. Adjusting the VCO free running frequency using the potentiometer will not cause the two signals to "fall out of synchronization". Instead, you will just shift the phase (time delay) between the reference signal and the output signal.

If your circuit fails to synchronize the signals rock solid, you probably have calculated the wrong filter constants, have forgotten to block the DC level of the reference input signal (a 0 to 5 V signal has a 2.5 V DC component), or have exceeded the maximum input voltage for the reference signal (± 1 V).

SESSION 27: Demodulation of Frequency Shift Keying (PSK)

In this lab the "error" voltage of the phase locked loop (the VCO control voltage) will be used to recover high-low voltage type binary signals from high-low frequency type signals.

(1) Reconstruct the FSK "data" generator of Lab 24.

(2) Design and build a PLL circuit which tracks the attenuated signal from (1). The difference between the error voltage on the PLL pin 7 and the reference on pin 8 should be filtered and compared. The output of the comparator will reproduce the 60 Hz "data". Remember that the dc component of the pin 7 voltage can be adjusted (when the loop is locked) by adjusting f_0 with the tuning resistor. Such an adjustment will probably be necessary to allow your 60 Hz "data" to switch the comparator.

SESSION 24: THE 566 Voltage Controlled Oscillator And Frequency Shift Keying

Use the 566 VCO to generate a signal which changes from 2000 Hz to 2200 Hz (5% accuracy) and back again 60 times per second. (Normally, of course, the. frequency. changes are caused by binary data not the line frequency.) Power this circuit from the ± 6 volt supplies you constructed in Lab 12.

Save either this circuit, or all details about this circuit, for use in Lab 27. By powering this circuit from ± 6 volts you have made the interfacing to Lab 27 much easier.