

A High Gain Amplifier

Given the limitations of our breadboard, we first have to set up a suitable input signal for this lab session. Before you venture into this part of the lab exercise, you should review the handling instructions for CMOS devices on Page 6-6 of the lecture notes.

We will use the CD 4029 presetable up/down counter to divide the frequency of the 100 kHz breadboard clock signal by a factor of 8, as the 100 kHz is too fast and the 1 kHz is too slow for our purpose. Fig.1 shows how to connect the CMOS chip, and the circuit you should use to get an appropriate input signal from the CD 4029 output. The network of two capacitors and two resistors following the presetable counter converts its high amplitude (5V) square wave output into a low amplitude (2mV peak-to-peak) triangular wave signal with no DC offset. Be aware that 2 mV peak-to-peak is not easy to see on your scope. This low amplitude, 12.5 kHz triangular wave output signal of the circuit below is the input signal that you are to amplify with in your circuit.

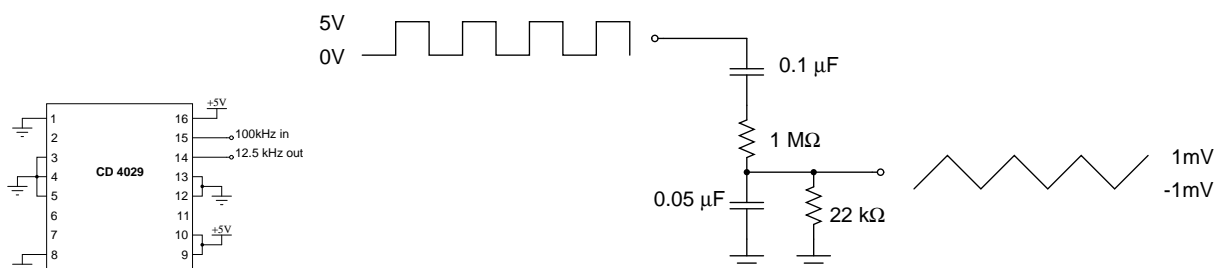


Figure 1: Generating the input signal

Your **task** is to amplify this output signal to a peak-to-peak amplitude of (1.0 ± 0.25) V, maintaining the triangular shape of the waveform with no DC offset. Also you should definitely look at the “open loop voltage gain vs. frequency” curve in the data sheets of your op-amp (shown on the 351 data sheet, not 741), try to build your circuit in a way that it does not depend on a specific op-amp being used. Your TA may test you there by changing the op-amps on your board. Your gain should not be affected by this action, i.e. should not depend on the individual gain of the specific op-amp you chose out of your selection. As usual your records should fully document all calculations that go into your design. And of course you will have to be able to explain how your design works.

Three more comments to guide you:

First you need to consider what the loading by your input stage does to the output stage of the input signal generating circuit that you set up above. You may want to design a “buffer” for the first stage of your amplifier, yet with the proper caution that should not really be necessary.

Second you do not want to have any offset voltage on small signals. You may be forced to null offsets on any amplification stage that has small input signals.

Third you may be tempted to build your amplifier and go for a gain of 500 in one fell swoop. Is that wise? The answer to this question feeds directly into the loading of your input stage...