

Write your name at the top right corner of every page (including this cover page).

Copy everything you want counted towards your grade onto the pages that I provided.

Write with a pen that cannot be erased!

No books or calculators are allowed!

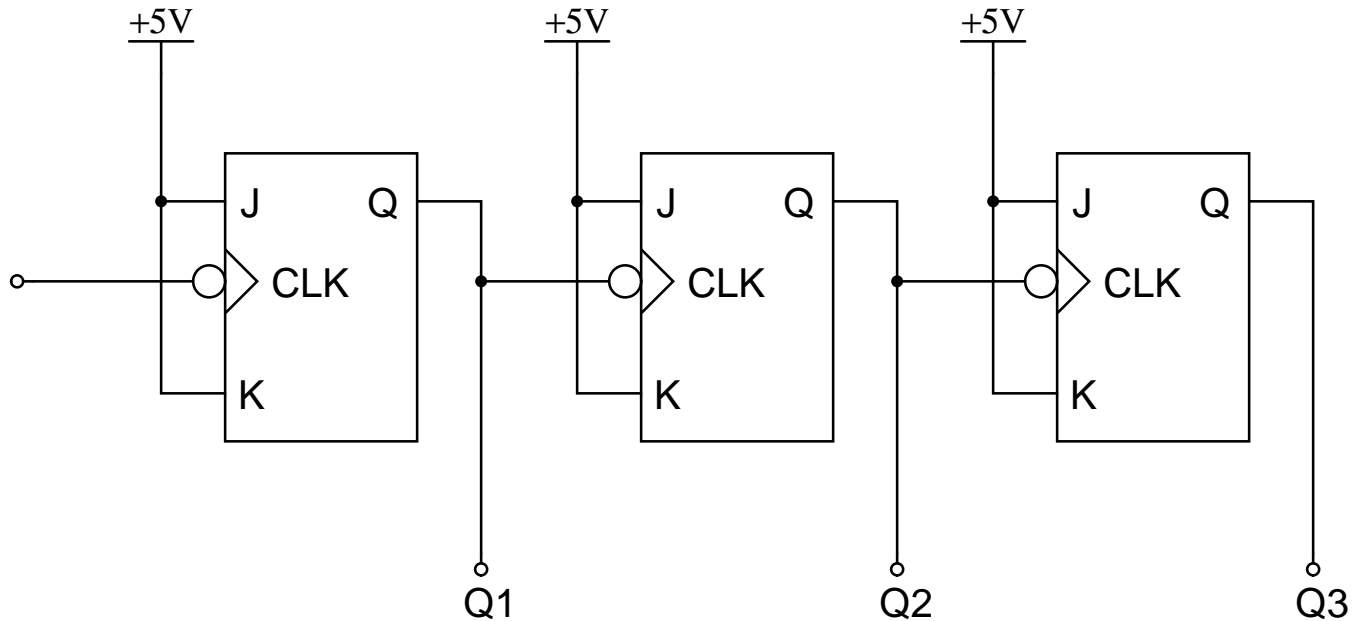
Write down all the steps that lead to your result.

Identify new variables that you may introduce in the circuit diagrams that I provided.

Read all the problems before you start so that you can begin with those that seem easiest to you.

Problem 1 (7 pts):

For the circuit shown: Complete the table below of sequential states as they change from one clock edge to the next:

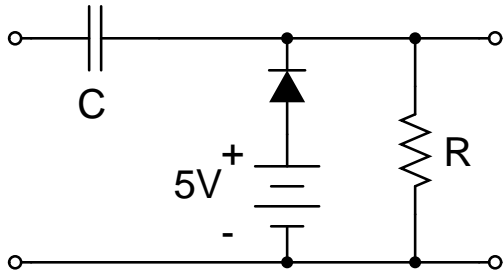


The triangle at the clock input tells you that you are looking at edge-triggered flip-flops. The negation circle in front of the triangle means that you are looking at a flip flop that triggers on the negative edge (falling). So the output state changes on every negative edge of the clock signal:

	Q1	Q2	Q3
first:	0	0	0
next:	1	0	0
next:	0	1	0
next:	1	1	0
next:	0	0	1
next:	1	0	1
next:	0	1	1
next:	1	1	1

Problem 2 (8 pts):

Draw a circuit diagram for a circuit that would clamp a sinusoidal input waveform to sit on top of a +5V offset. Remember to make sure a current can always flow. Do not count on the load for this. If you use a diode, assume it is ideal - no forward voltage drop. With an ideal diode: does your circuit impose a restriction on the frequency of your input sinusoid? What is that restriction?

Solution:

In order for this to work the time constant of the circuit needs to be $RC \gg \omega^{-1}$.

Problem 3 (8 pts):

Write the Karnaugh map and analyze it to find an efficient(!) implementation for the following truth table; derive the logic expression as a sum of products and draw the resulting circuit diagram:

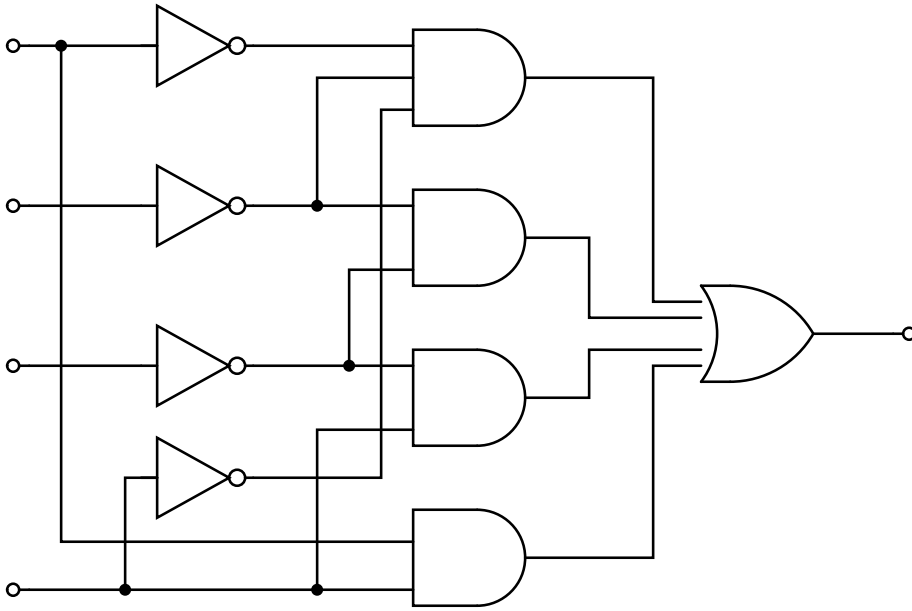
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Solution: The Karnaugh map is:

AB CD	00	01	11	10
00	1	1	0	1
01	0	1	0	0
11	0	1	1	0
10	1	1	1	0

Be sure to get the order right: Only one bit changing between rows or columns!

$$F = \overline{A}\overline{B}\overline{D} + \overline{B}\overline{C} + \overline{C}D + AD$$

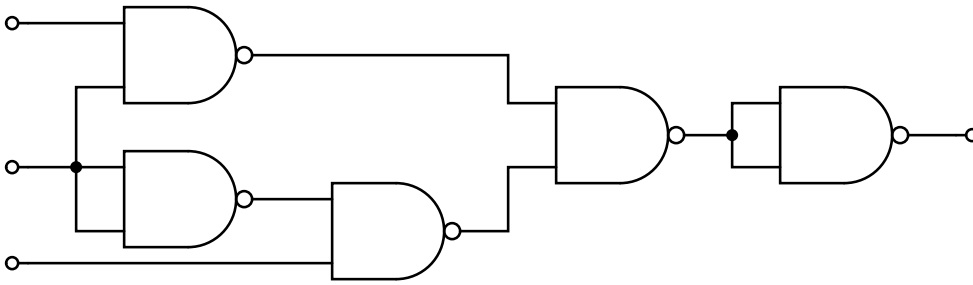


Problem 4 (6 pts):

Implement the logic function $F = (\overline{A} + \overline{B})(B + \overline{C})$ purely through NAND gates.

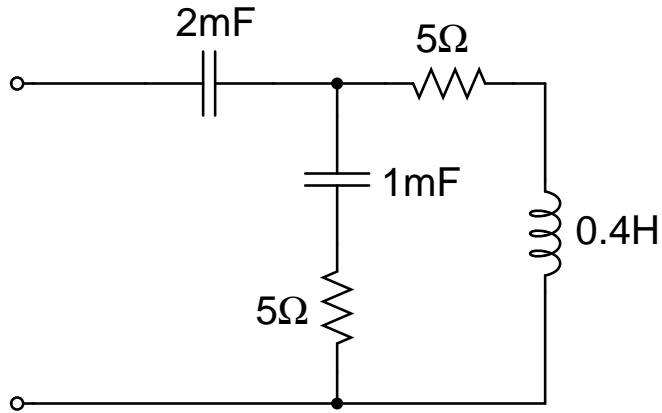
Solution:

De Morgan yields: $F = (\overline{AB})(\overline{BC})$



Problem 5 (8 pts):

Find the input impedance of the following circuit at 50 rad/s:



Solution: At 50 rad/s the impedances of the components are: 1 mF $\Rightarrow -j20\Omega$, 2 mF $\Rightarrow -j10\Omega$, and 0.4 H $\Rightarrow j20\Omega$.

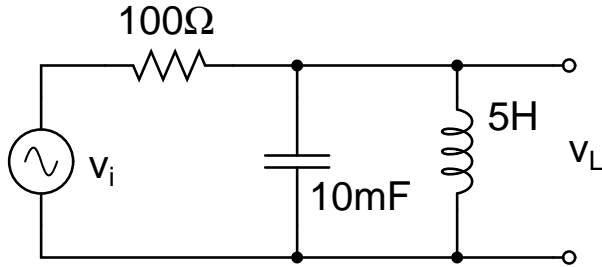
Therewith: $Z_1 = -j10\Omega$, $Z_2 = 5\Omega - j20\Omega$, $Z_3 = 5\Omega + j20\Omega$, and

$$Z_{in} = Z_1 + (Z_2 || Z_3) = Z_1 + \frac{Z_2 Z_3}{Z_2 + Z_3}$$

$$= (-j10 + \frac{(5-j20)(5+j20)}{(5-j20)+(5+j20)})\Omega = (-j10 + \frac{25+400-j(100-100)}{10})\Omega = (42.5 - j10)\Omega \text{ at } 50 \text{ rad/s}$$

Problem 6 ONLY 6610 students !!! (8 pts):

Determine v_L in the following circuit if $v_i = \sqrt{0.5} \sin(4 \text{ rad/s } t + \phi)$ with $\phi = 45$ degree:



After bringing the sine wave into cosine form, the input is $v_i = \sqrt{0.5} \cos(4 \text{ rad/s } t - \phi)$, so the corresponding phasor is $(\sqrt{0.5}, -45)$ [angle in degree] and its respective complex component representation is $(0.5 - j0.5)V$. At 4 rad/s the impedances are: $Z_C = -j25\Omega$ and $Z_L = j20\Omega$. The two are in parallel and we are interested in the voltage across this parallel impedance of:

$$Z_2 = \frac{Z_L Z_C}{Z_L + Z_C} \Omega = \frac{-j25 \times j20}{-j25 + j20} \Omega = j100\Omega$$

This is in series with a $Z_1 = 100\Omega$ resistor and therefore the output voltage is:

$$V_L = \frac{Z_2}{Z_1 + Z_2} V_i = \frac{j100}{100 + j100} V_i = (0.5 + j0.5) V_i = \sqrt{0.5} e^{j45} V_i$$

$$\text{Thus: } \mathbf{V}_L = \sqrt{0.5} e^{j45} (\sqrt{0.5}, -45) = (0.5, 0)$$