Operational Transconductance Amplifier

Recall the OpAmp

In a OTA replace the VCVS with a VCCS

Furthermore: $g_m$ is a function of $I_{ABC}$ (amplifier current)

Need two things to understand CA3080
- Differential Pair (long-tailed pair)
- Current Mirrors (current sources)
Properties of CA3080

\[ g_m = 19.2 \left( \frac{I_{ABC}}{\text{mA}} \right) \mu \text{S} \]

\[ R_{out} = \frac{7.5 \text{ k\Omega}}{I_{ABC} / \text{mA}} \]

Linearity of \( \frac{g_m}{I_{ABC}} \): \( I_{ABC} \in [0.5 \text{ mA}, 500 \mu \text{A}] \)

60 dB!

How to get \( I_{ABC} \): (a diode above \( V_- \))

\[ V_m \frac{R_m}{R_m+R_p} \text{ or } V_- \]

\[ I_{ABC} = \frac{V_m - V_-}{R_m} \]

Voltage Gain

- Need load!

\[ G = \frac{V_{out}}{V_{in}} = \frac{I_{out} R_L}{V_{in}} = g_m R_L \]

Gated Unit-Voltage-Gain Amplifier

\[ I_{ABC} = 500 \mu \text{A} \rightarrow g_m = 10 \text{ m}\mu \text{S} \]

\[ G = 100 \]

\[ V_{out} = V_{in} \text{ by symmetry to } 1\% \]
Sample-and-Hold Circuit

\[ V_{out} = V_c = V_s \quad \text{if} \quad \frac{\partial V_s}{\partial t} \ll \frac{1}{RC} \]

\[ V_c < V_T \quad V_c \text{ frozen} \]

(eventually leakage current will kill it)

With the CA3030

"Emitter" follower with huge input impedance

When "off" \( V_c \) is "held"
FET Amplifiers (Common Source)

Like BJT, have to bias first.

\[ I_{ds} \] and \[ V_d \] both vary from device to device!

Issues:

If \( R_s = 0 \), possibly in cut-off (want active)

If \( V_{gs} = 0 \) \((R_s \neq 0)\) consider load line

\[ I_d \] \( \frac{V_{gs}}{R_s} \]

\[ V_{gs} = -I_d R_s \]

Can reduce uncertainty by moving away from origin!
Can now also work with enhancement MOSFET’s

Bias Recipe

1. Pick $I_D$
2. Determine $V_{GS}$ from $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$
   or $I_D = \frac{K}{V_T} (V_{GS} - V_T)^2$

3. Remember $V_{DS} > V_G - V_P$ for active! (Pick $V_{GSS}$)
4. Need a particular gain? Another constraint
   Then pick $R_S, R_D$
FET small-signal model: y-model

Use voltages as independent parameters

\[ i_o = \frac{\partial I_{out}}{\partial V_{in}} \bigg|_{V_{out}} V_o + \frac{\partial I_{out}}{\partial V_{out}} \bigg|_{V_{in}} V_o \]

\[ i_i = \frac{\partial I_{in}}{\partial V_{in}} \bigg|_{V_{out}} V_o + \frac{\partial I_{in}}{\partial V_{out}} \bigg|_{V_{in}} V_o \]

\[ i_o = y_o v_i + y_o v_o \]

\[ i_i = y_i v_i + y_i v_o \]

For common-source

\[ i_o = y_{os} v_i + y_{os} v_o \]

\[ i_i = y_{is} v_i + y_{os} v_o \quad \Leftarrow \text{ignore at small } \omega \]

\[ v_i = v_{gs} \quad v_o = v_{ds} \]

\[ i_o = i_d \]

\[ g_m = \frac{i_d}{v_{gs}} = \frac{i_o}{v_i} = y_{fs} \]

\[ g_d = g_{out} = \frac{v_o}{i_o} = \frac{v_{ds}}{i_o} = \frac{1}{y_{os}} \]

\[ i_d = i_o = g_m v_{gs} + \frac{1}{g_d} v_{ds} \]
Complimentary MOSFET Logic (CMOS)

Use NMOS & PMOS pairs with identical characteristics

Inverter

(Using enhancement MOSFETs, OFF at $V_{DS} = 0$)

\[ I_D = I_{DS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \]

\[ g_m = \frac{dI_D}{dV_{GS}} = -\frac{2}{V_P} \sqrt{I_D I_{DSS}} \]

\[ g_m \approx g_m(V_{GS} = 0) = -\frac{2 I_{DSS}}{V_P} \]

\[ g_m = g_m \sqrt{\frac{I_D}{I_{DSS}}} \]
Case 1 $v_{in} = 0$: $M_1$ OFF
$M_2$ ON

$V_{GS2} = -V_{DD} < -\alpha$

$V_{out}$ floats up to $V_{DD}$

Case 2 $v_{in} = V_{DD}$: $M_2$ OFF
$M_1$ ON

$V_{out}$ floats down to 0

NAND Gate

NOR Gate