Digital Device Review

Two voltages
Noise Margin: $V_{Hi} - V_{LO}$ $V_{LO} - V_{Hi}$

Logic Gates
Buffer
NOT
AND
NAND
OR
NOR

Truth Tables

Boolean Algebra - Logic Functions

2-Input Functions

\[
\begin{array}{cc|cc}
A & B & 0 & 1 \\
\hline
0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

EX-OR

\[
\begin{array}{cc|cc}
A & B & 0 & 1 \\
\hline
0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 \\
\end{array}
\Rightarrow
\begin{array}{cc|cc}
A & B & 0 & 1 \\
\hline
\overline{A} & \overline{B} & 0 & 1 \\
0 & 0 & 0 & 1 \\
0 & 1 & 1 & 1 \\
1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

\[A + B = \overline{AB} + \overline{A}B + AB\]

\[
\begin{array}{c}
\downarrow \\
B = A + B
\end{array}
\]
How to add 1 or 2 inputs?
(To get 3 input functions)

Consider \[ B = \begin{pmatrix} A^B \\ 0 \\ 0 \end{pmatrix} \]

Need to keep 1s together
Unwrap

\[
\begin{array}{cccc}
AB & 00 & 01 & 10 \\
\hline
0 & 0 & 1 & 1 \\
1 & 0 & 0 & 0
\end{array}
\]

Then add another line (or two)
(usually put A separately)

Example: \[ F = \overline{ABC} + ABC + \overline{ABC} + \overline{ABC} + \overline{ABC} \]

<table>
<thead>
<tr>
<th>ABC</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>0</td>
</tr>
<tr>
<td>010</td>
<td>0</td>
</tr>
<tr>
<td>011</td>
<td>1</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>101</td>
<td>1</td>
</tr>
<tr>
<td>110</td>
<td>1</td>
</tr>
<tr>
<td>111</td>
<td>1</td>
</tr>
</tbody>
</table>

This is a Karnaugh Map
Solving Karnaugh Maps

1. Represent $F$ as a sum of minterms (ie. as a truth table)

2. Place outputs in map

3. Group adjacent “1s” in groups of $2^n$ from largest to smallest.
   Groups can “wrap around”

4. Stop when each 1 is in a group

   (or)

5. Simplified result is sum of groups

\[
\begin{array}{c|c}
1 & 00 \\
1 & 01 \\
0 & 11 \\
0 & 10 \\
\end{array}
\]

8 - nothing
4 - 2nd row
2 - 3rd column
Done

2nd row $\rightarrow A$
3rd column $\rightarrow BC$

\[F = A + BC\]
Four variables example

\[
\begin{array}{|c|c|c|c|}
\hline
\text{A} & \text{B} & \text{C} & \text{D} \\
\hline
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 1 & 0 & 1 \\
0 & 1 & 1 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 \\
1 & 0 & 1 & 0 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
1 & 1 & 0 & 1 \\
1 & 1 & 1 & 0 \\
1 & 1 & 1 & 1 \\
\hline
\end{array}
\]

\[
F = \overline{BC} + \overline{B} \overline{CD} + \overline{AB} \overline{D}
\]

it is not

\[
F = \overline{BC} + \overline{B} \overline{CD} + \overline{AB} \overline{CD}
\]

(which has one extra!)

Digital IC's (MSI, LSI, VLSI)

We use TTL & CMOS IC's

Already known: \( V_H \), \( V_L \), \( V_{HI} \), \( V_{LO} \)

For TTL powered at 5V

\[
\begin{align*}
V_H &= 0.8 \quad V_L = 0.4 \\
V_{HI} &= 2.0 \quad V_{LO} = 2.4 \\
\text{Noise margin} &= 0.4 \text{ V}
\end{align*}
\]

Also currents:

\[
\begin{align*}
I_H &= I_L \\
I_{HI} &= I_{LO}
\end{align*}
\]

\text{\&} and "Fanout" for TTL \( PO = ^{\sim}10 \)

\[
\begin{align*}
I_{H0} &= 4.0 \mu A \\
I_{L0} &= 1.6 \text{ mA (sink)}
\end{align*}
\]

Ex: using TTL NAND as NOT

\[
\begin{array}{|c|}
\hline
\text{\overline{DO}} \\
\hline
\end{array}
\]

\[
\begin{align*}
\text{\overline{DO}} &= \frac{V_{HI}}{I_H} = 500 \Omega \\
\end{align*}
\]

"Floating" TTL inputs will rise above \( V_{HI} \) (not recommended)
FOR CMOS

Power $V_{DD}$ $V_{SS}$

$V_{DD} = S$ (usually for $V_{DD}$)

$V_{SS} = 0$

$V_{IL} = 0.45 \ V_{DD}$

$V_{IH} = 0.55 \ V_{DD}$

$V_{IL} \leq 0.3 \ V_{DD}$

$V_{IH} \geq 0.7 \ V_{DD}$

I vary small

F0 large

Must connect all inputs ($V_{DD}$ or $V_{SS}$)

---

Sequential Logic
Logical Systems with "States"

SR Flip-Flop

Consider this system

```
S  \hline
   \downarrow 1
   \uparrow\downarrow\uparrow
   \hline
R  \hline
```

Construct $TT$

Suppose $Q=1$, $S=R=0$

NOR 1 $S+\bar{Q} = \bar{Q} = 0$

NOR 2 $R+\bar{Q} = Q = 1$ Stable
<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>\overline{Q}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Not allowed</td>
</tr>
</tbody>
</table>

Clocks & Gates

Often want to restrict changes to certain times: Say if S or R takes on intermediate values and we want to make sure they're 1 or 0.

Gated NAND SR FF
D-type FF

\[ D \xrightarrow{\text{SR}} Q \]

\[ Q \leftarrow D \text{ on CLK} \]

Timing Diagrams

Draw logic state vs time

CLK

SR FF

\[ S \]

\[ R \]

\[ Q \]

\[ \overline{Q} \]

More Feedback

Expect:

CLK

\[ Q \]

\[ \overline{Q} \]
Get:
\[ \text{clk} \]
\[ 0 \quad \text{high} \quad \text{while} \quad \text{true} \]

Race Conditions!
\[ Q \rightarrow \overline{Q} \rightarrow Q \quad \text{as fast as possible} \]
while Gate is on!

Two Solutions

Master-Slave

\[ \text{clk} \]
\[ \text{signal} \]
\[ Q_1 \]
\[ Q_2 \]

Edge Trigger
State can only change
when CLK edge goes up
(or down)
JK F/F

Add input to feedback D F/F

State only oscillates when J=1

More general:

Note: S=R=1 is impossible.

TT for JK F/F

<table>
<thead>
<tr>
<th>Q0</th>
<th>Q0</th>
<th>J</th>
<th>K</th>
<th>S=JQ0</th>
<th>S=R=KQ0</th>
<th>Q1</th>
<th>Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>00</td>
</tr>
<tr>
<td>10</td>
<td>00</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>00</td>
</tr>
<tr>
<td>10</td>
<td>00</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>01</td>
</tr>
<tr>
<td>10</td>
<td>00</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>01</td>
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<td>01</td>
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<td>01</td>
</tr>
<tr>
<td>01</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>01</td>
<td>10</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

Sometimes for K doesn't matter.
\[ \begin{array}{c|c|c|c} Q_0 & J & K & Q_1 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \end{array} \]

Can restate \( T \) as excitation table

Give changes to state then cause

\[ \begin{array}{c|c|c|c} Q_0 & Q_1 & J & K \\ \hline 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \end{array} \]

**State Diagram**

Recall feedback D Flip-Flop

\[ \text{CLK} \quad 1 \quad 2 \quad 3 \quad 4 \quad 5 \quad 6 \]

\[ \text{N} \quad \text{Q} \]

\[ Q = N \mod 2 \]
Q is a clock with half the freq.!

CLK       D       0
           Q0
CLK       D       0
           Q1

1  2  3  4  5  6
CLK

Q0

Q1

11 10 01 00 00 10
3 2 1 0 3 2

This is a countdown timer
Same with JK or T F/F

Count up by using falling edge trigger