Session 3. Switched Capacitor Digital Filtering

In this Lab, you are to design a notch and bandpass filter using the MF10A switched capacitor filter. You will construct a filter with a high height-to-width ratio (Q). The filter will have a controllable centerpoint frequency $f_0$ (i.e., the position of the bandpass will be controllable through an external control signal.). Design the filter to have an $f_0$ which is switchable between 2 kHz and 20 Hz. You will use two different clock frequencies of your prototype board to control the $f_0$. The filter will have a Q of 20.

You should try to implement the filter using MODE 1 operation of the filter, outlined in Figure 7 of the Data Sheets (you can download these from the Physics 6620 web page under 'lab exercises' or also get it from www.national.com, search for MF10A). The chip should be run off ±6 V supplies, so you should use the LM7806 and LM7906 voltage regulators to provide this power, Note the LS input of the switched capacitor chip is attached to ground if the clock input is TTL compatible (like the protoboard square wave).

1) For the 1 kHz and the 100 kHz clock frequencies, feed a sine wave into the input of the filter and measure and plot the output amplitude (notch and bandpass) near the $f_0$ of each input frequency. Use the lab sine wave generator for the input, and do not exceed 250 mV p-p amplitude on the input to the filter.

2) Carefully examine the output response for frequencies in the range of 1/20 of the clock frequency up to 20 times the clock frequency. Are there any other gain bandpasses and/or gain notches in this frequency region? List the observed gain bandpass frequencies. Discuss how these gain bandpasses derive from the aliasing properties of the z-transform. Discuss how this affects the usefulness of the filter.